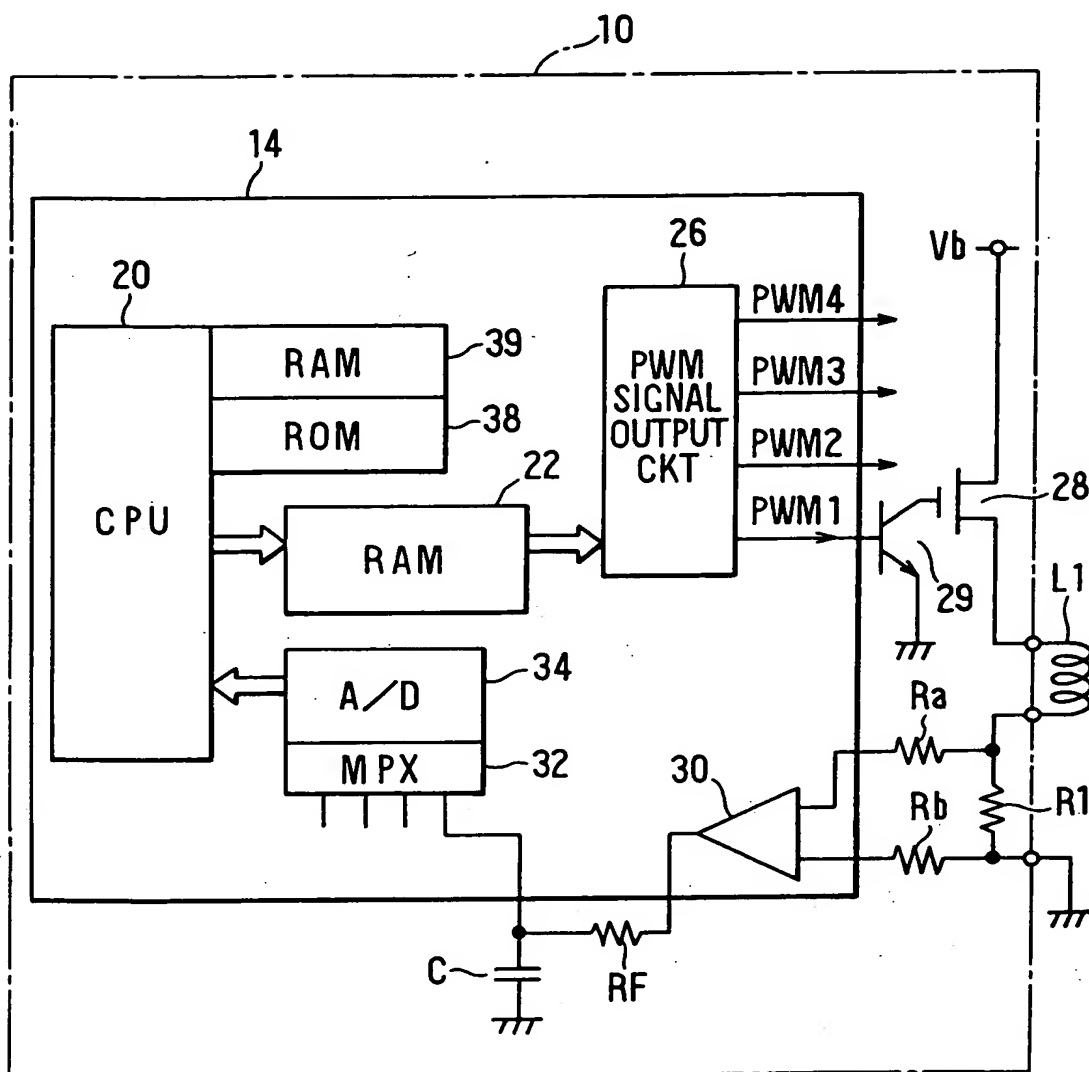


FIG. 1



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FIG. 2

RAM 22	
PWM1	CYCL(1)
	TON(1)
PWM2	CYCL(2)
	TON(2)
PWM3	CYCL(3)
	TON(3)
PWM4	CYCL(4)
	TON(4)

FIG. 3

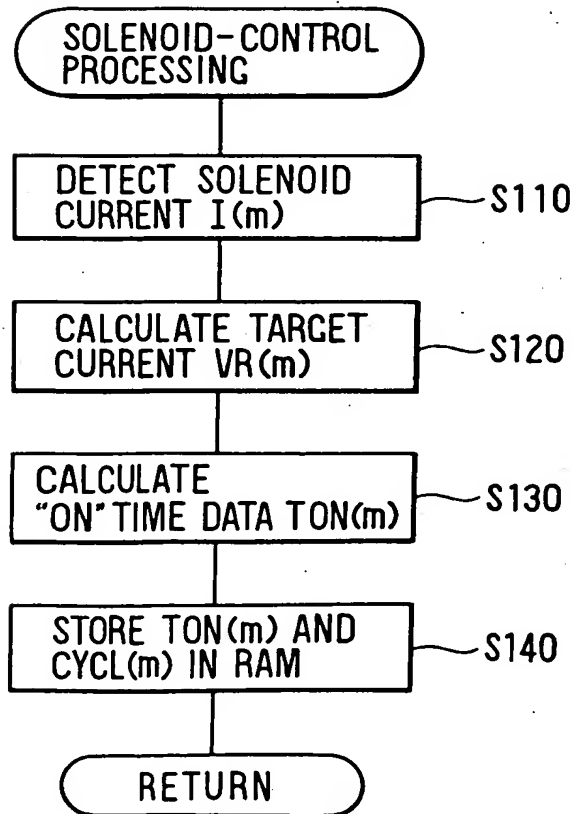
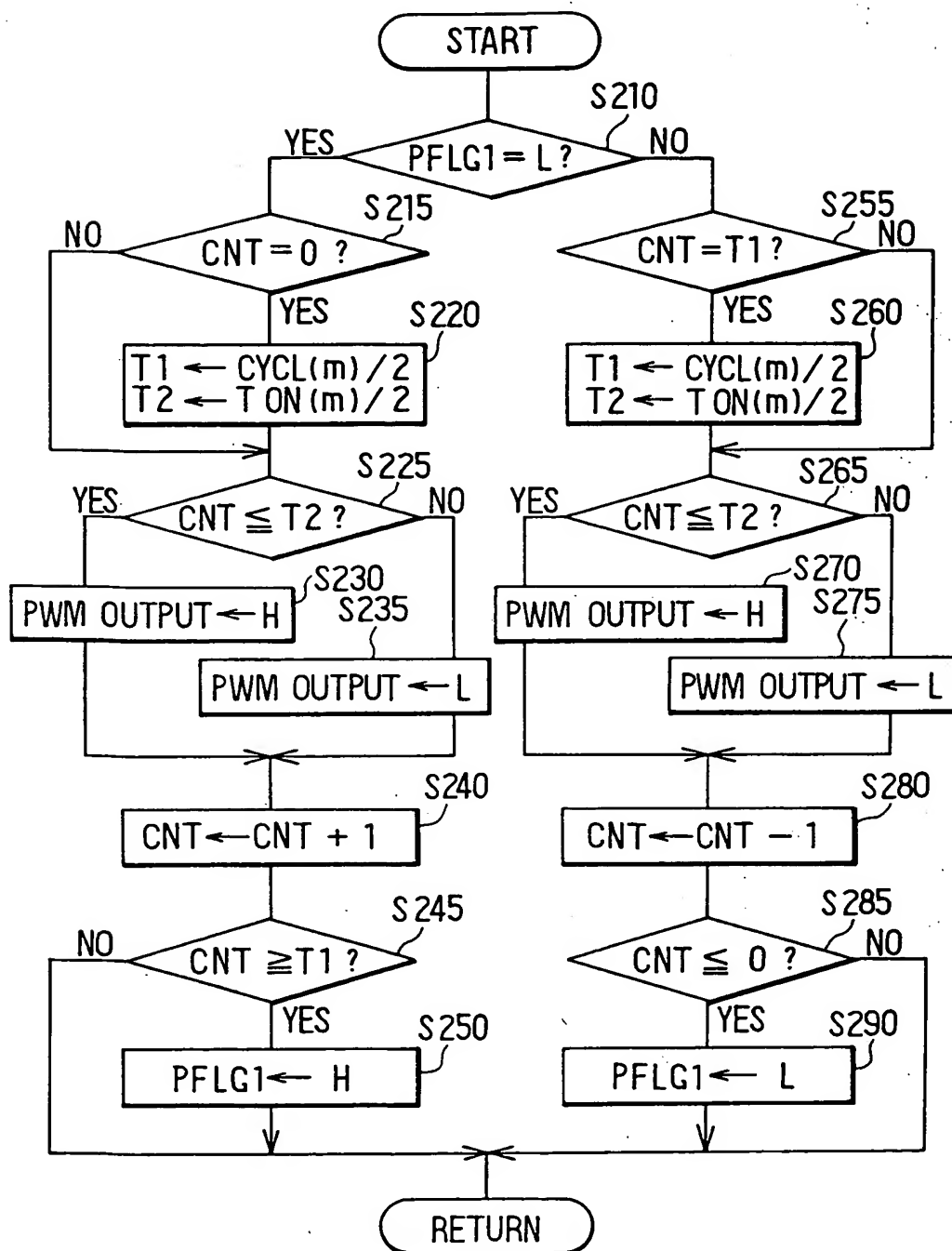
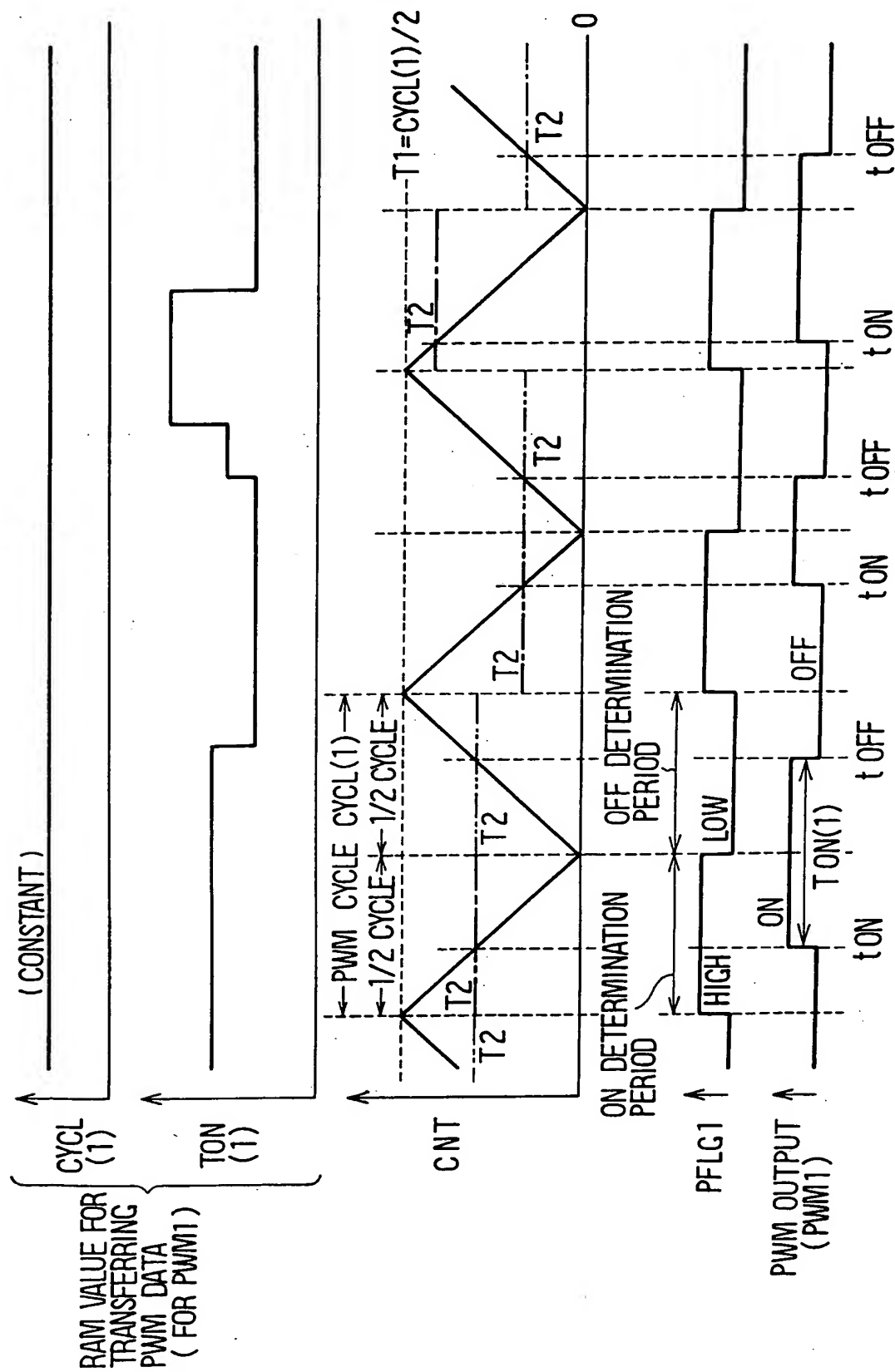


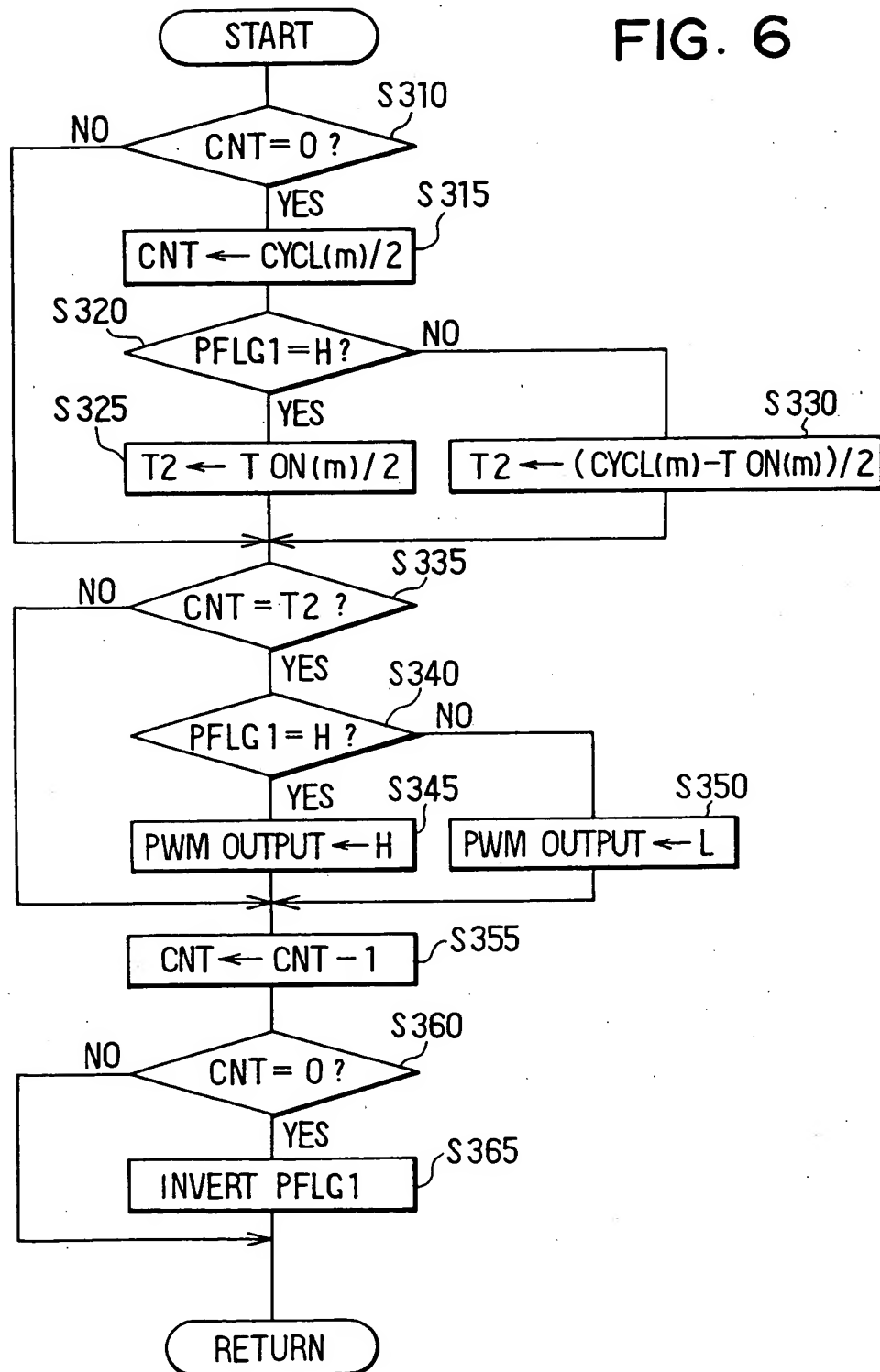
FIG. 4





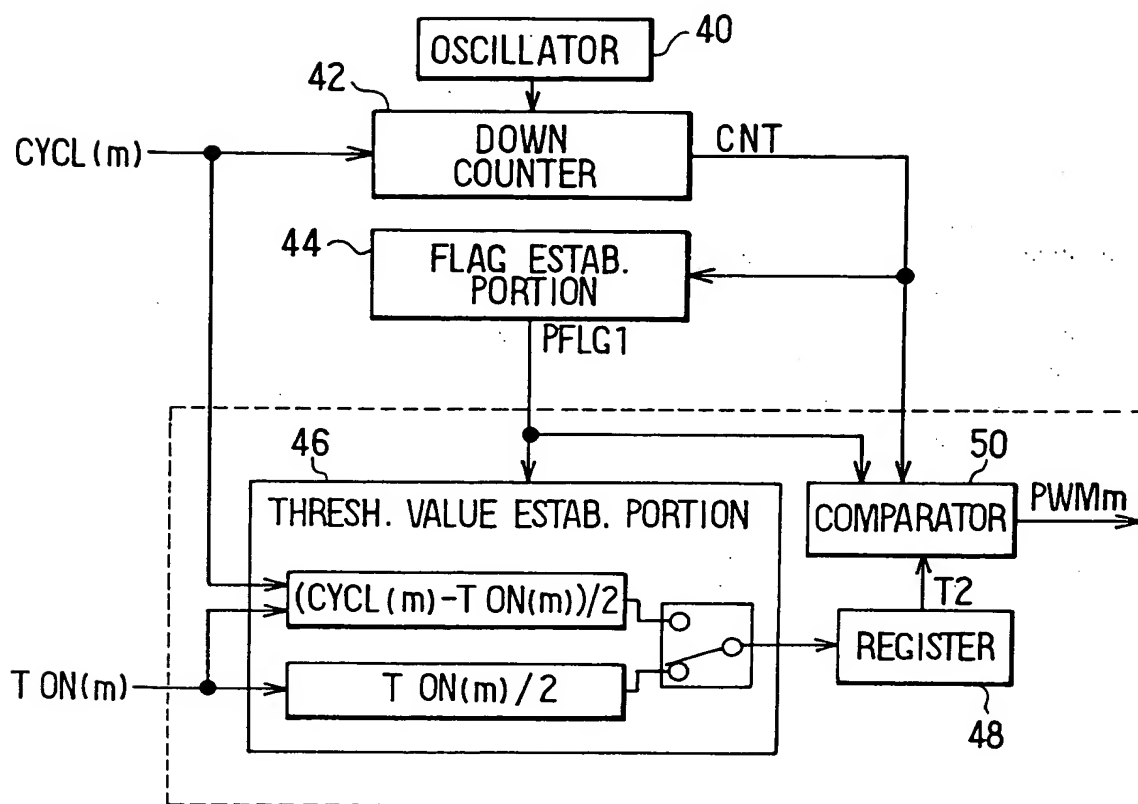
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FIG. 6



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FIG. 7



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FIG. 8

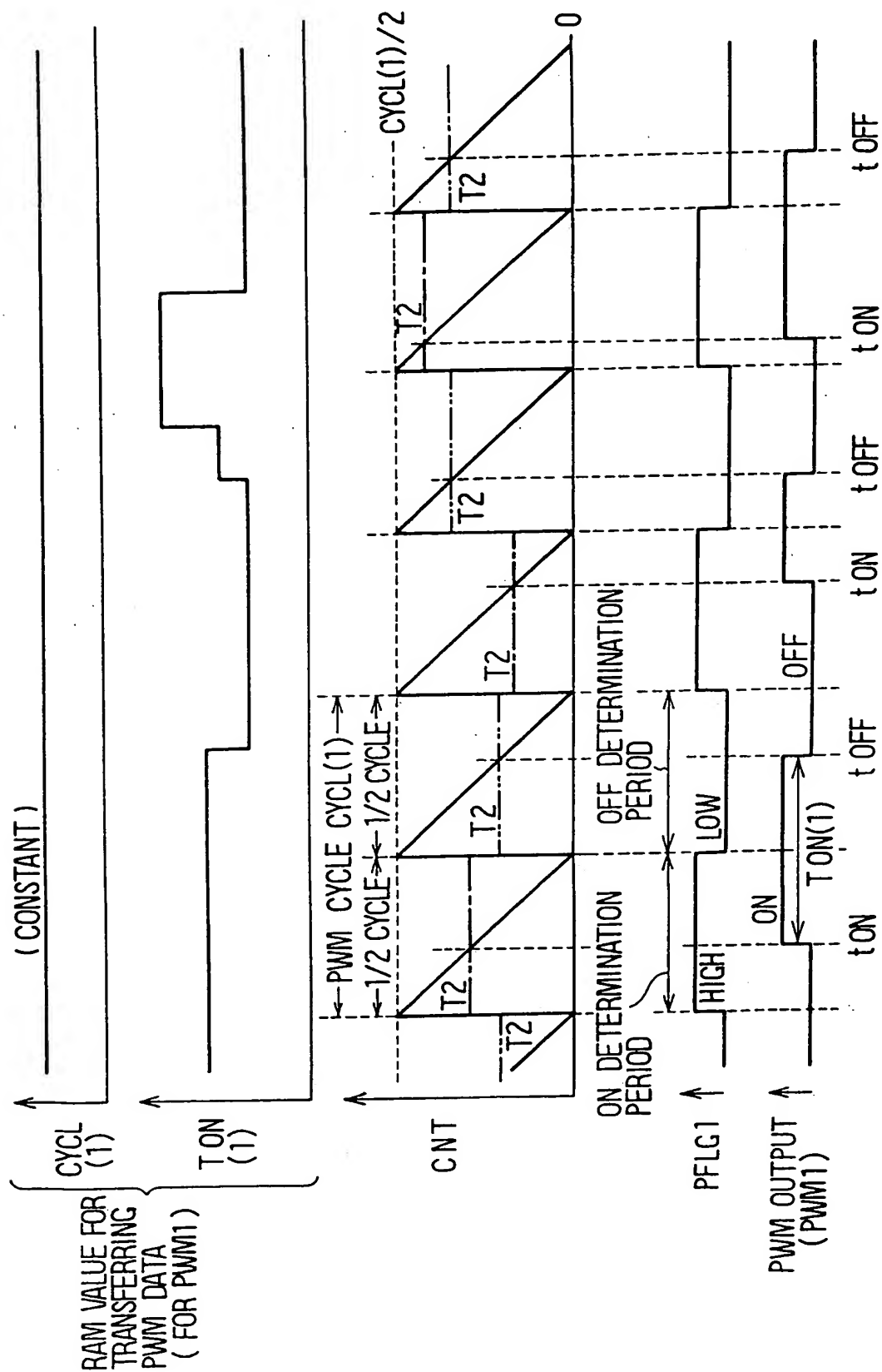
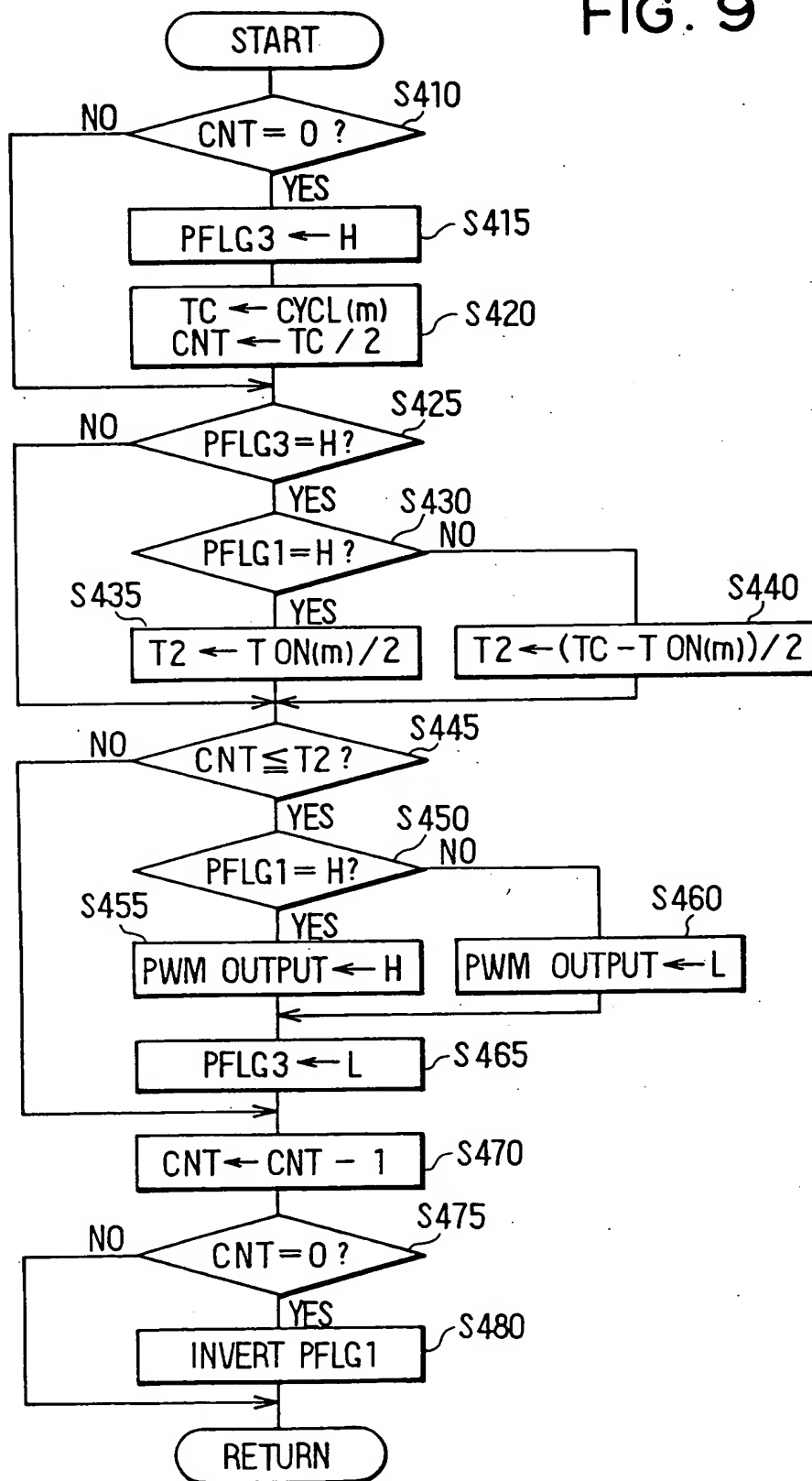


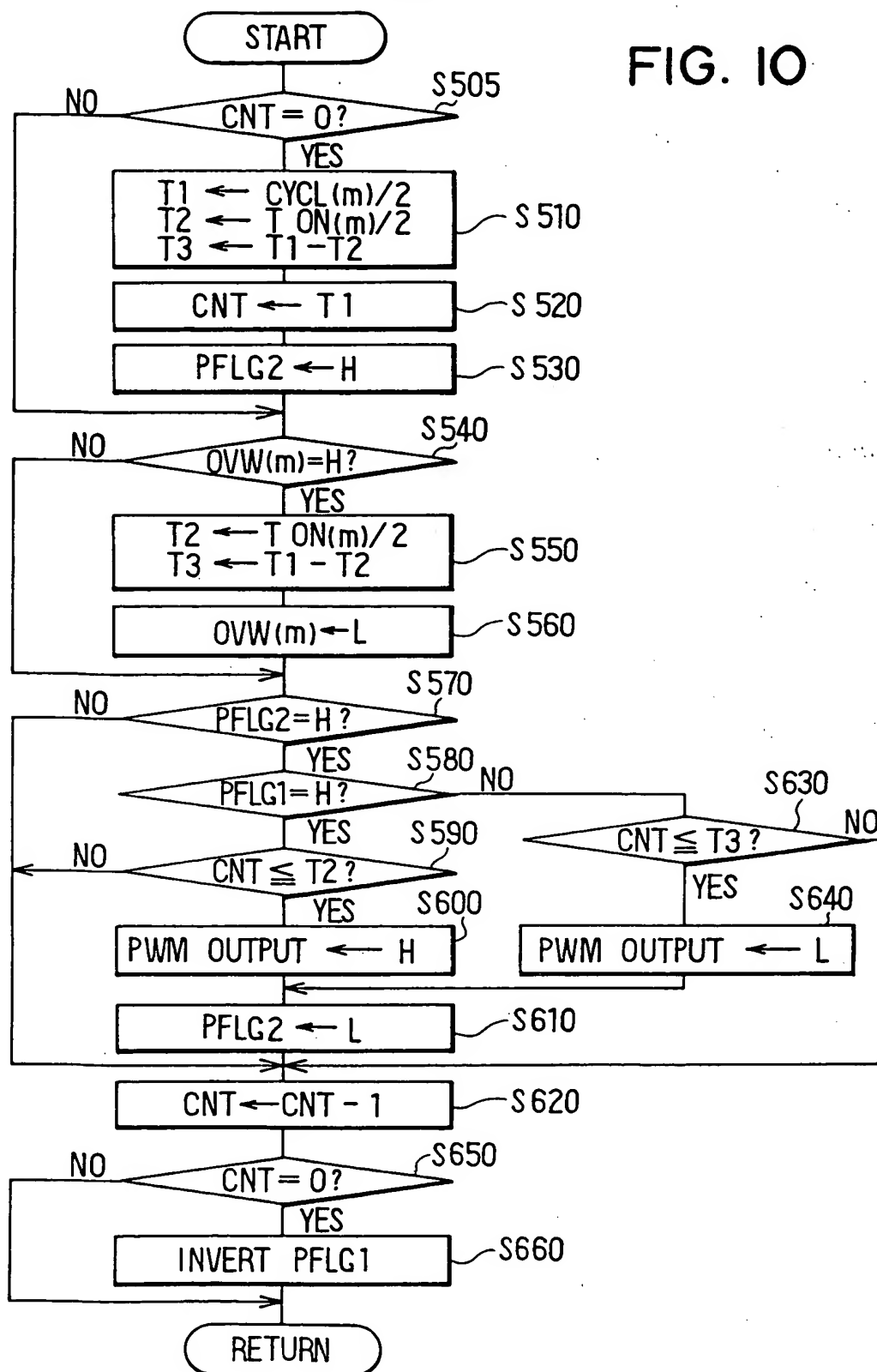
FIG. 9





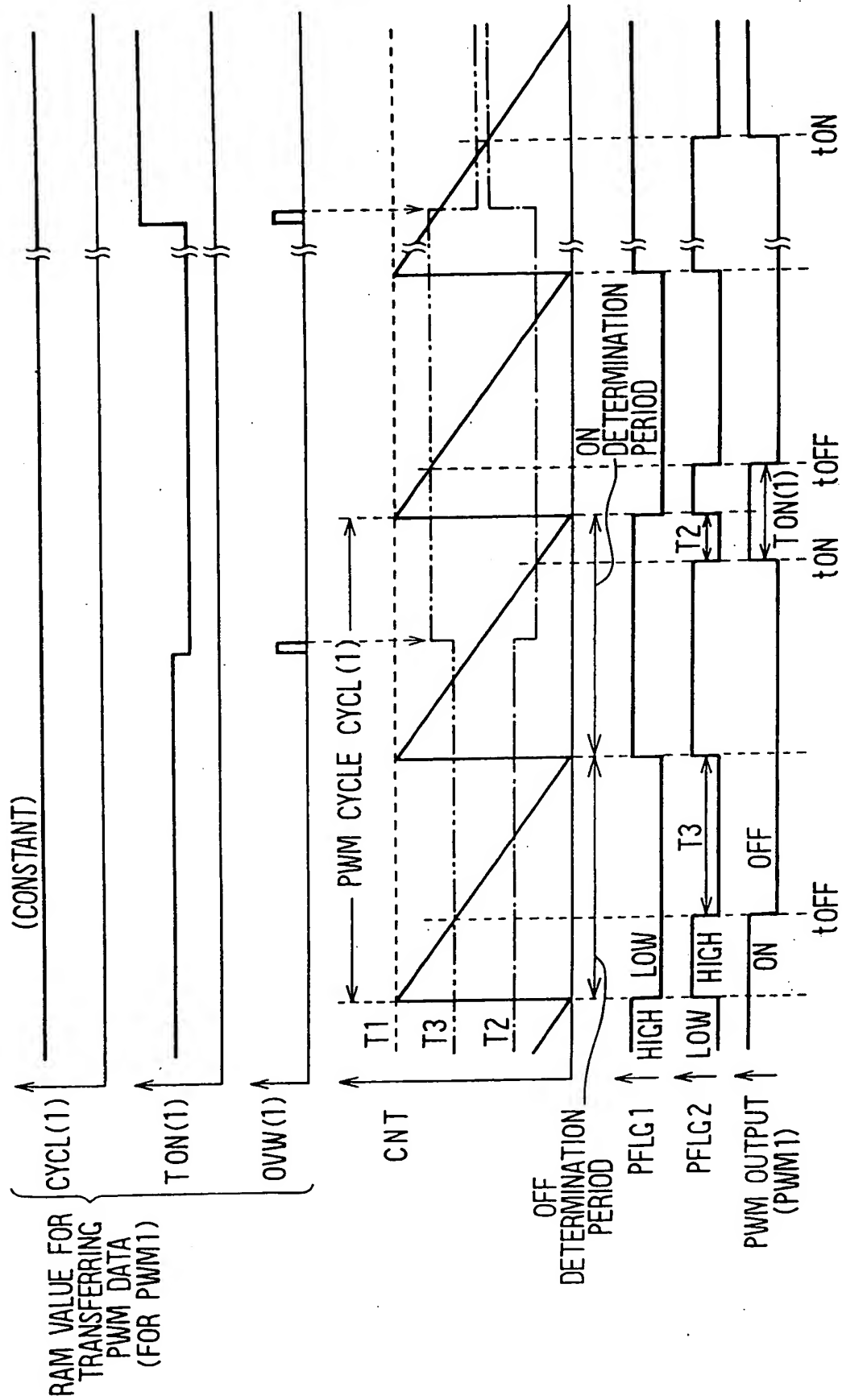
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FIG. 10



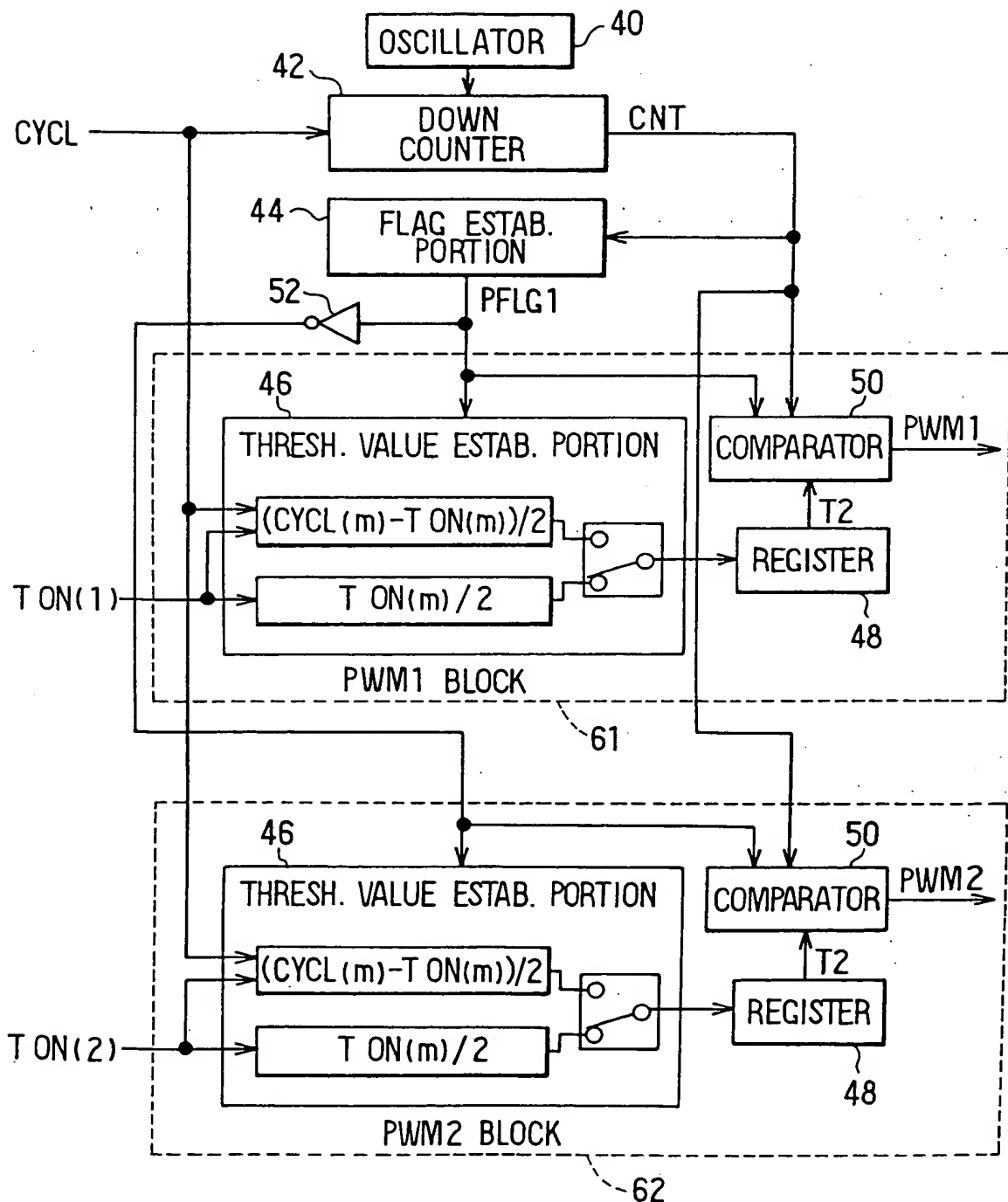
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FIG. 11



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FIG. 12



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FIG. 13

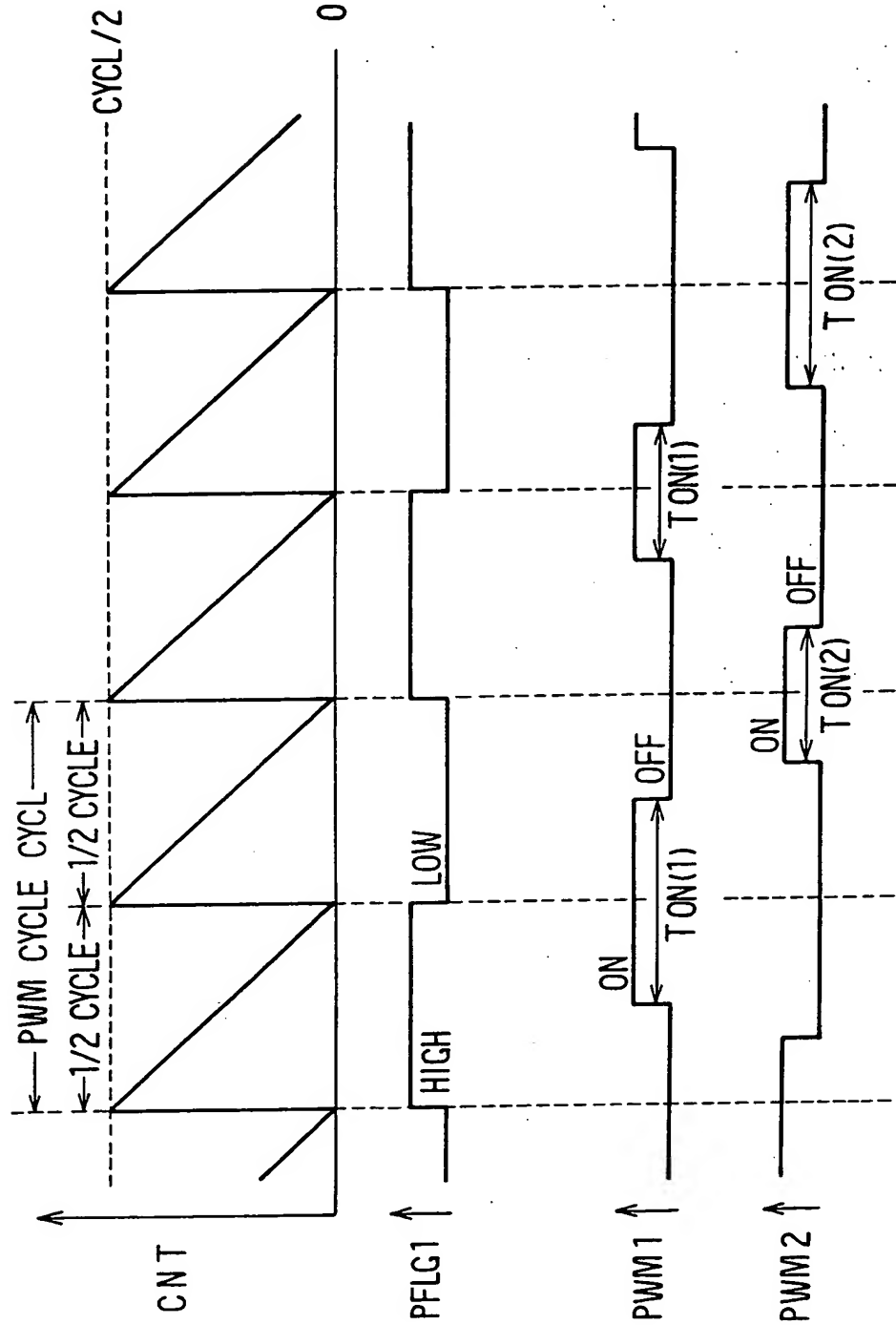


FIG. 14

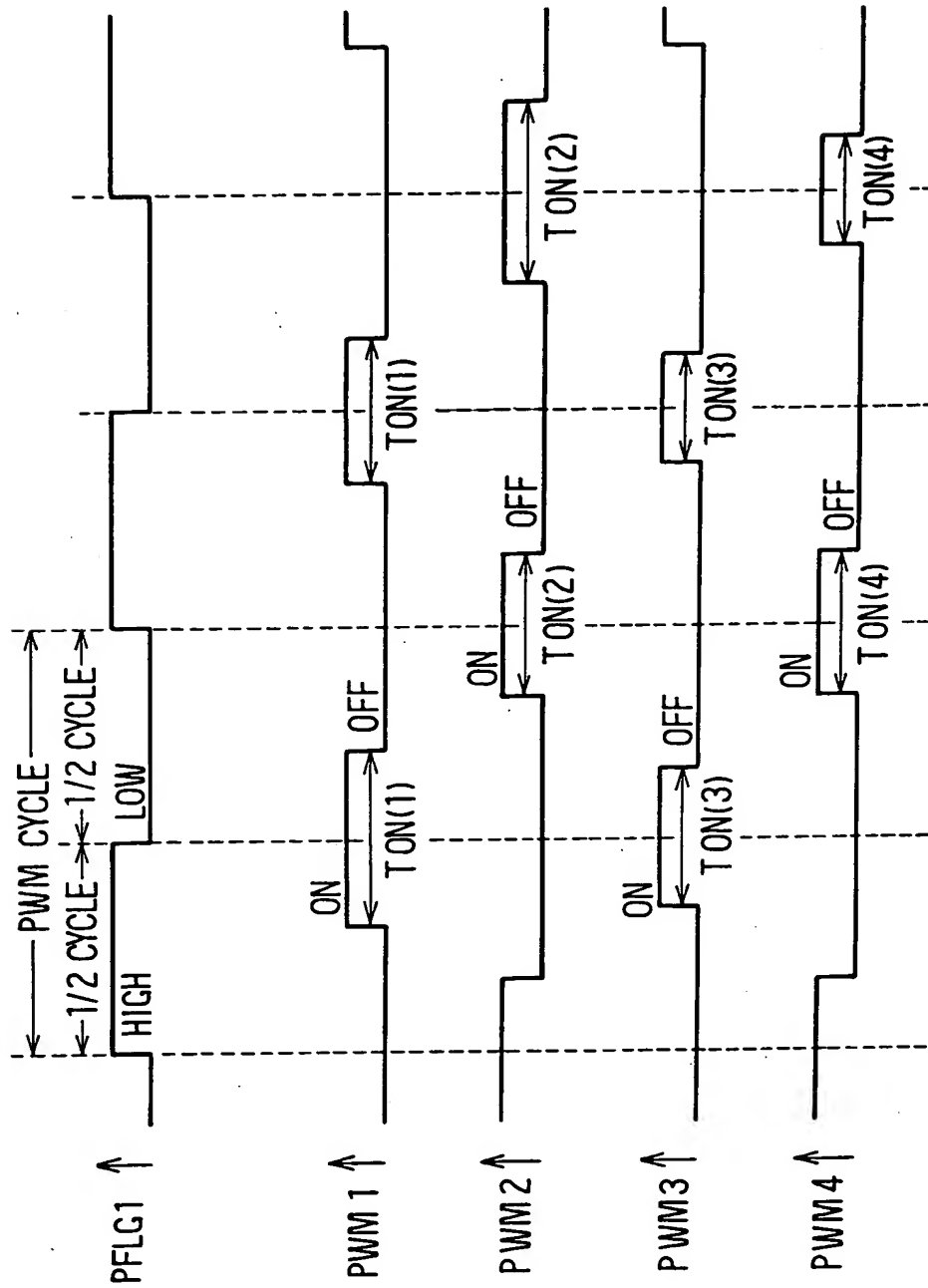
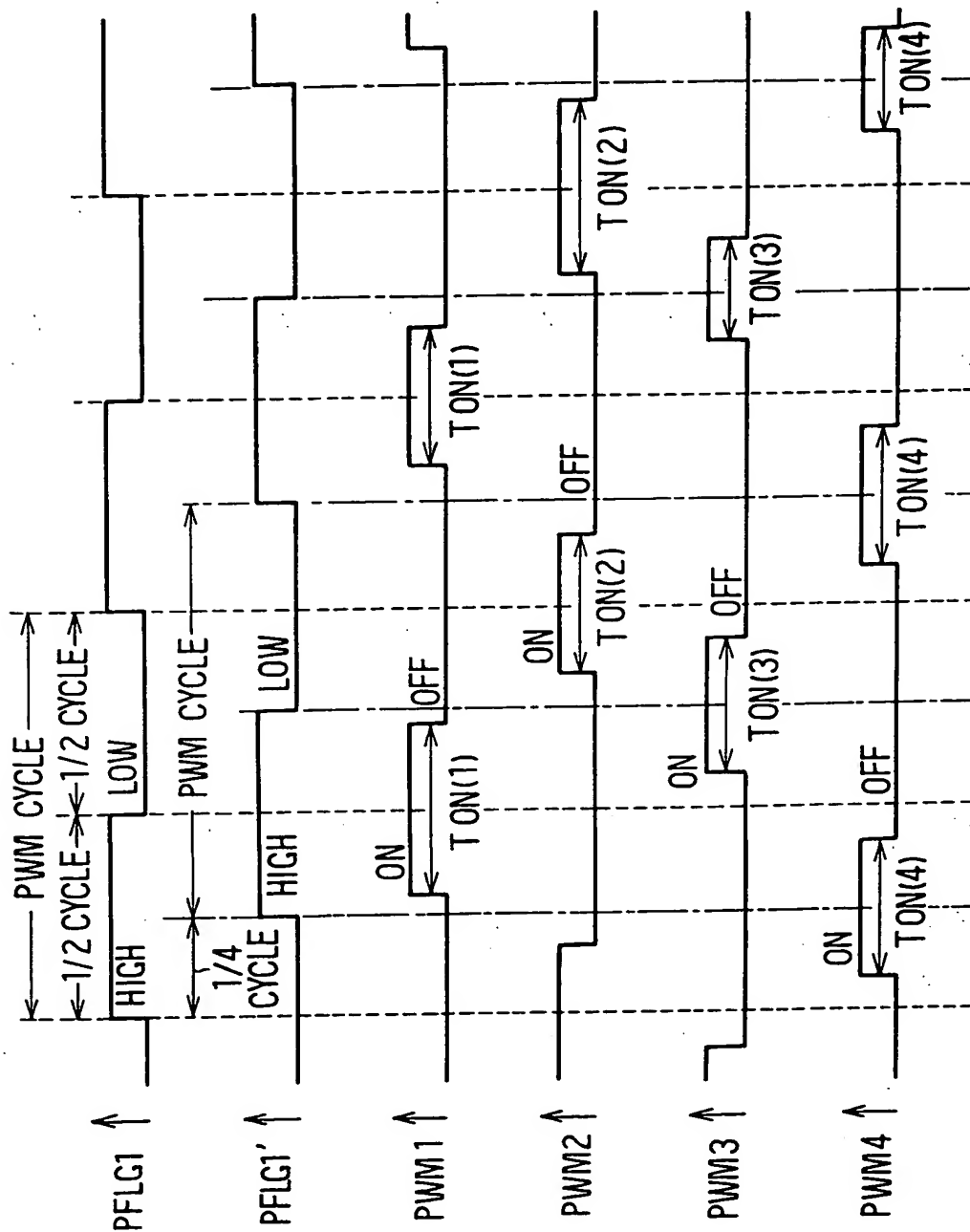
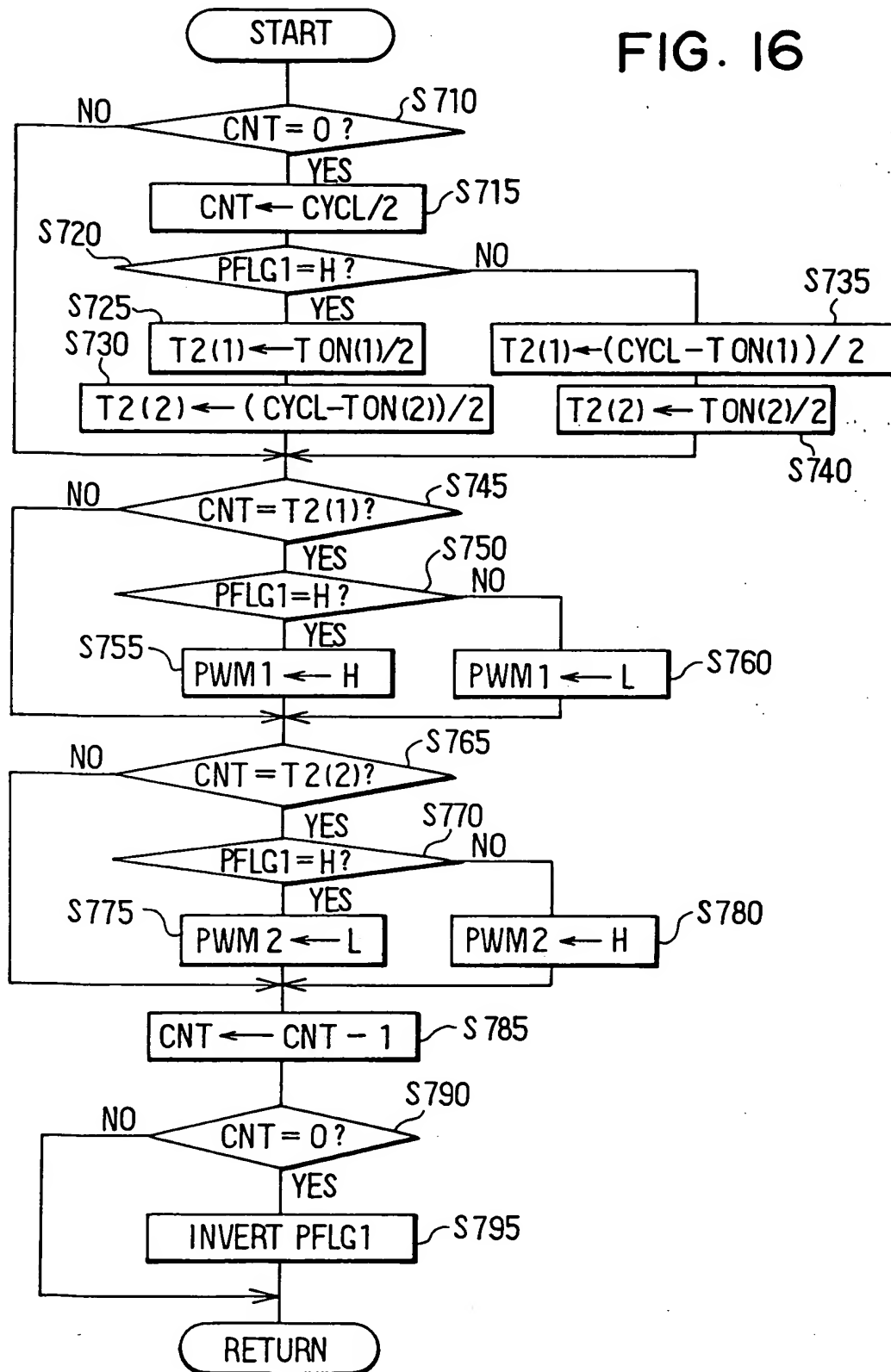


FIG. 15



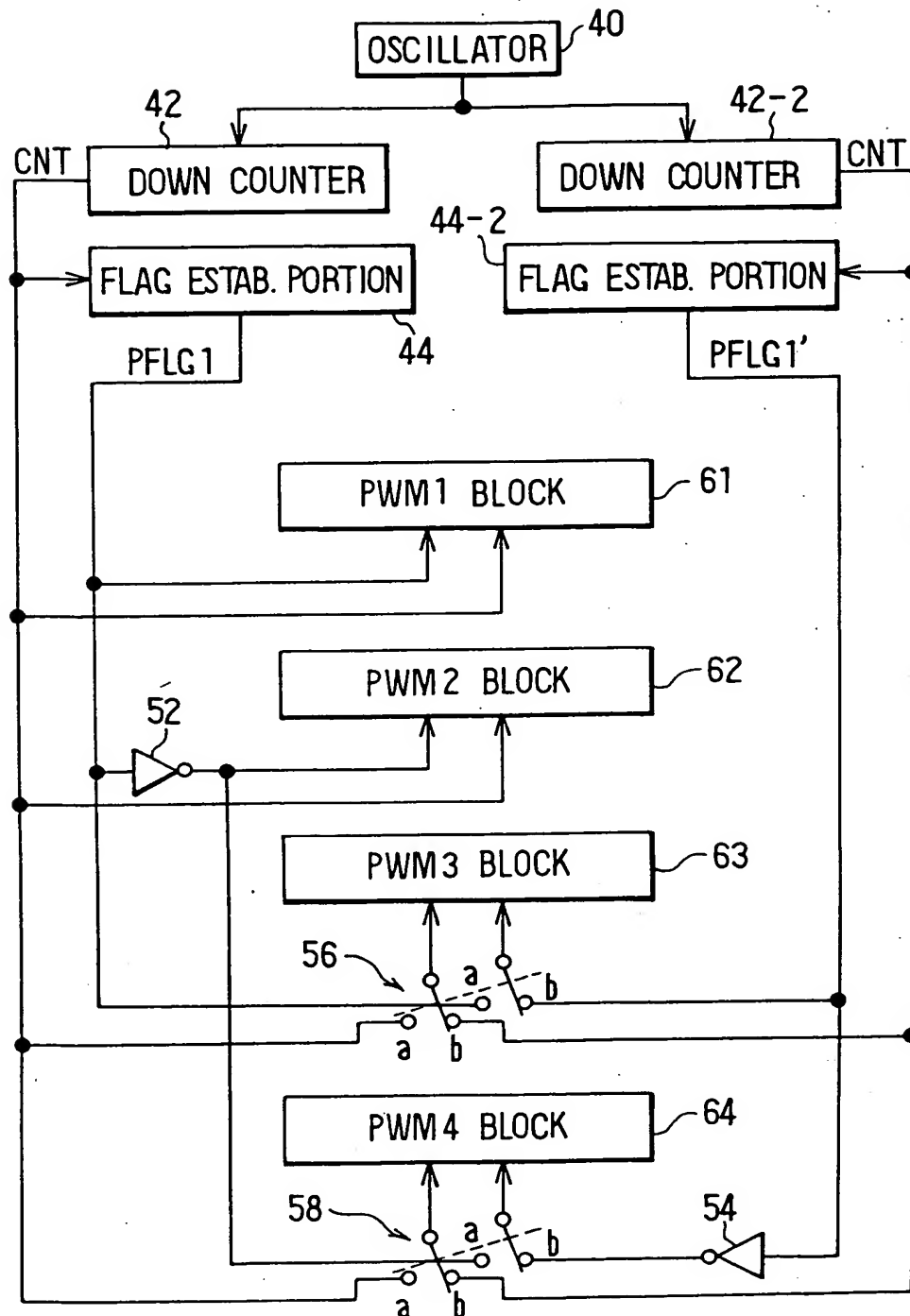
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FIG. 16



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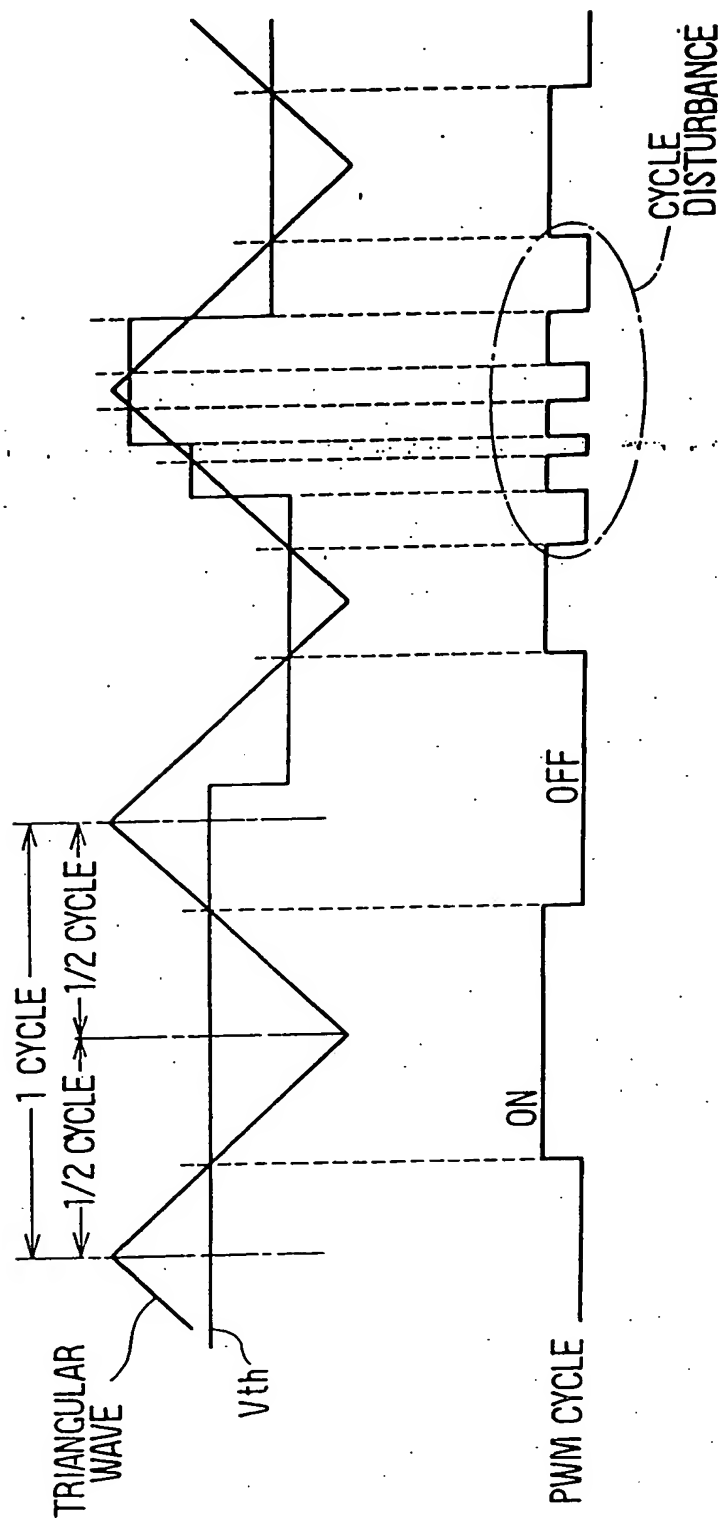
FIG. 17





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FIG. 18  
PRIOR ART



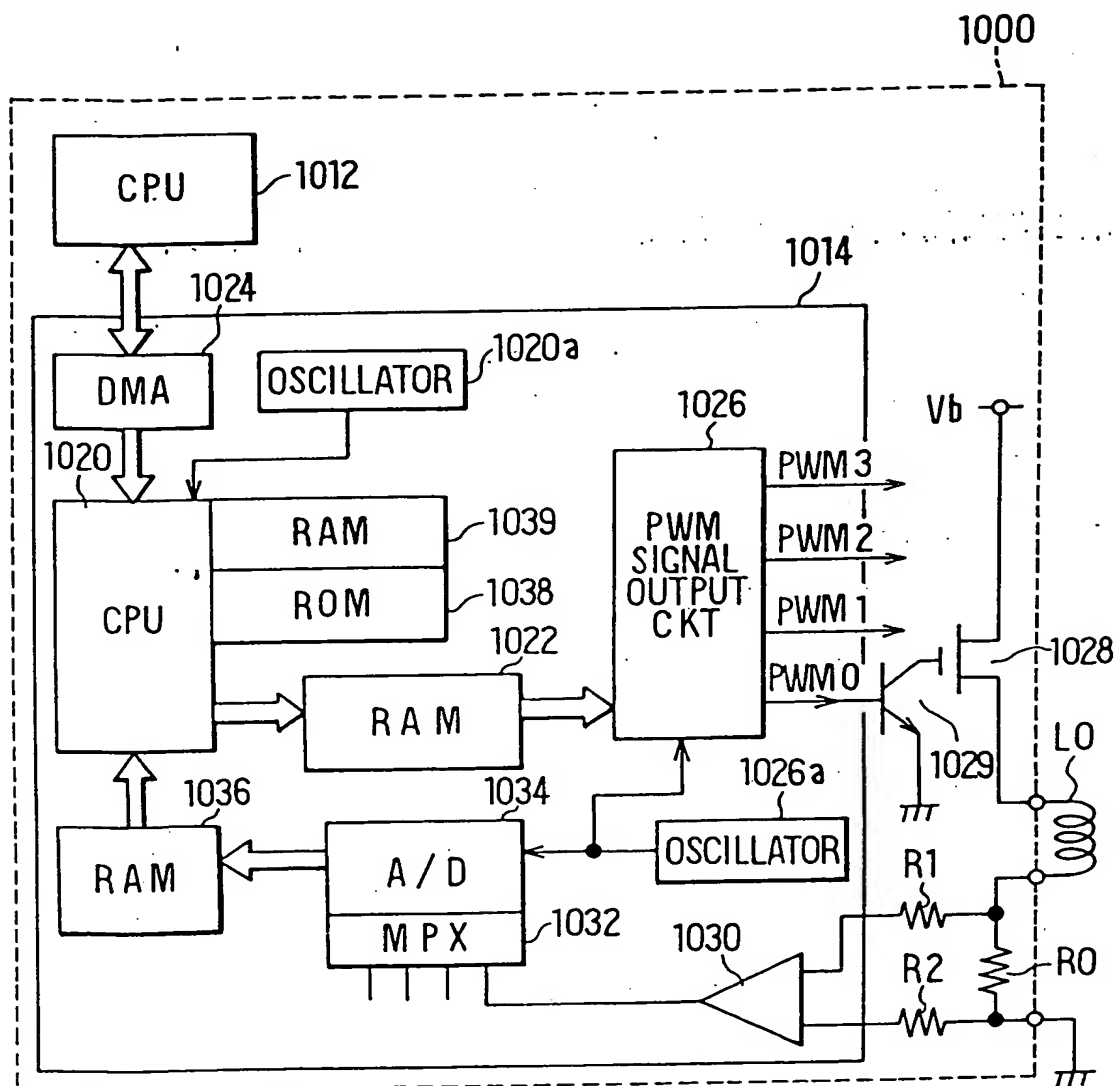


FIG. 20A

RAM 1022

PWM 0	CYCL(0)
	T ON(0)
	OVW(0)
PWM 1	CYCL(1)
	T ON(1)
	OVW(1)
PWM 2	CYCL(2)
	T ON(2)
	OVW(2)
PWM 3	CYCL(3)
	T ON(3)
	OVW(3)

FIG. 20B

RAM 1036

ch 0	ch 1	ch 2	ch 3
dat[0,0]	dat[1,0]	dat[2,0]	dat[3,0]
dat[0,1]	dat[1,1]	dat[2,1]	dat[3,1]
dat[0,2]	dat[1,2]	dat[2,2]	dat[3,2]
⋮	⋮	⋮	⋮
dat[0,14]	dat[1,14]	dat[2,14]	dat[3,14]
dat[0,15]	dat[1,15]	dat[2,15]	dat[3,15]

FIG. 20C

RAM 1034a

ch 0	ch 1	ch 2	ch 3
ad[0]	ad[1]	ad[2]	ad[3]

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FIG. 21

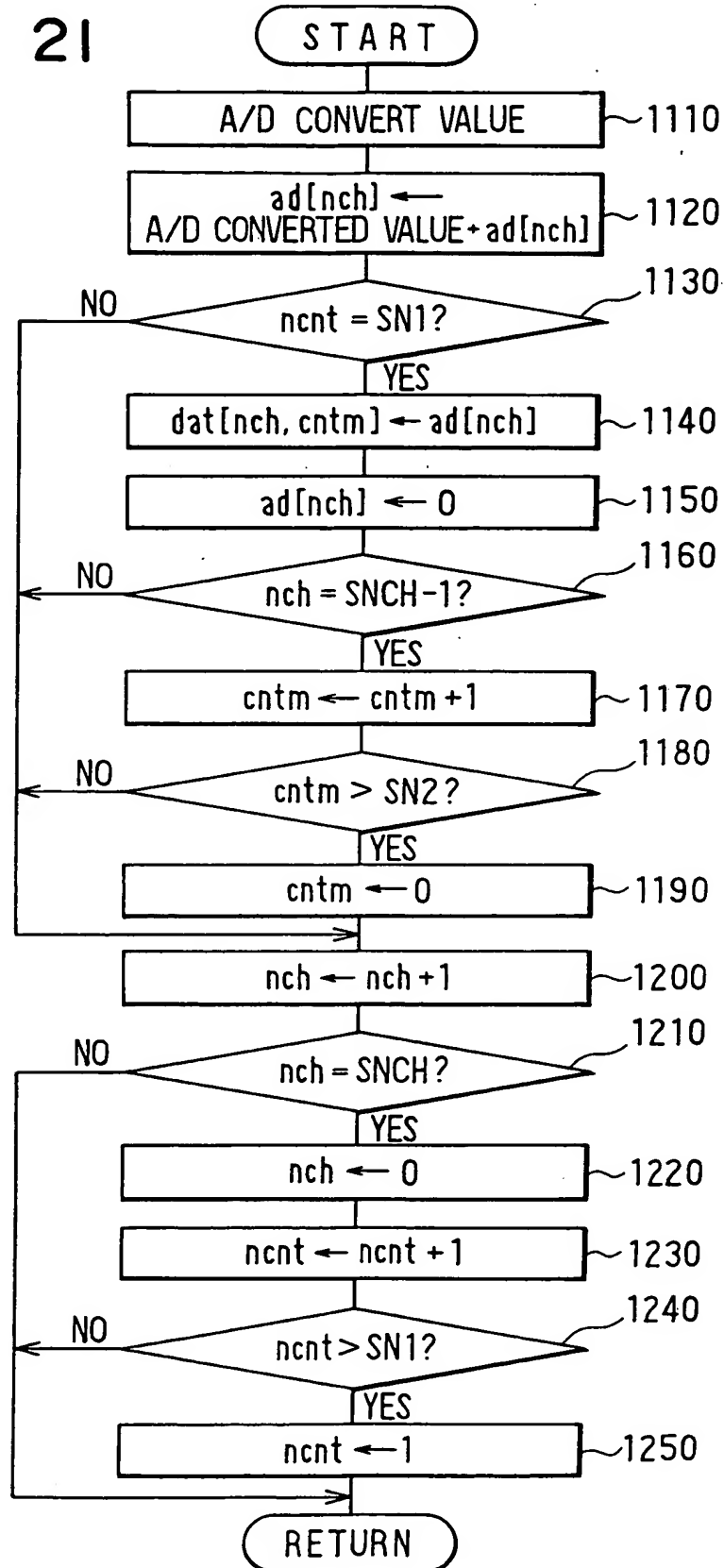
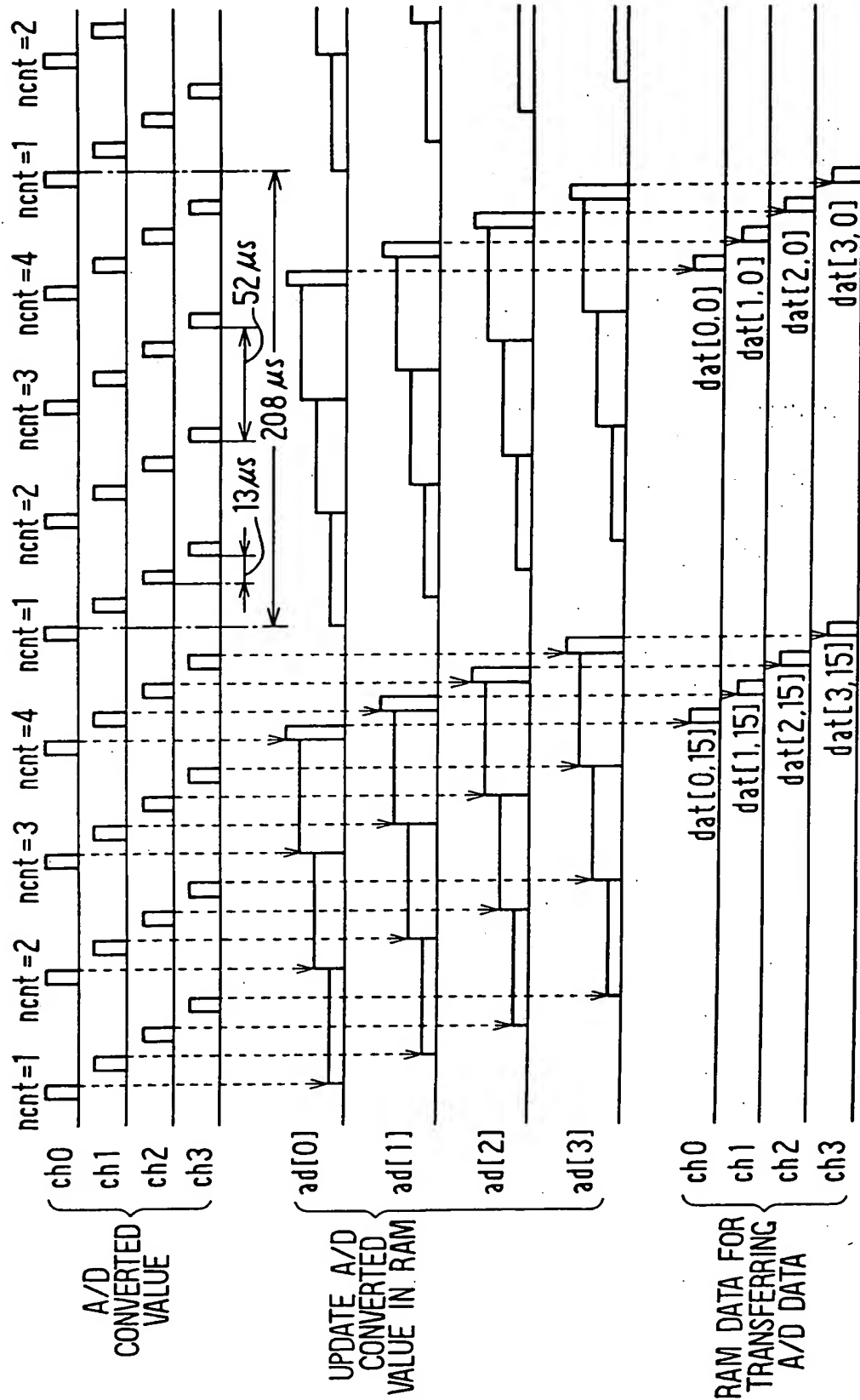


FIG. 22



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FIG. 23

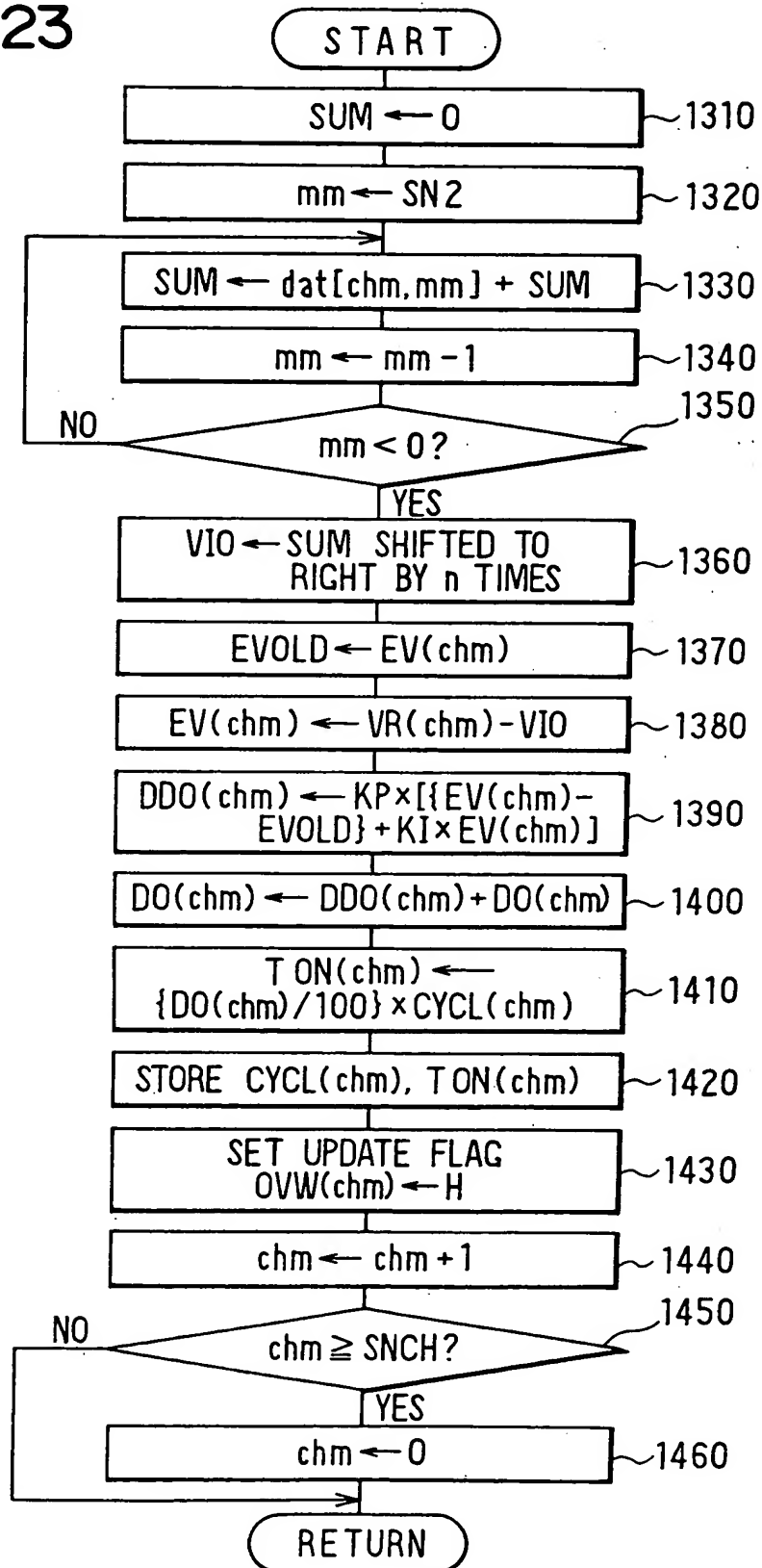


FIG. 24

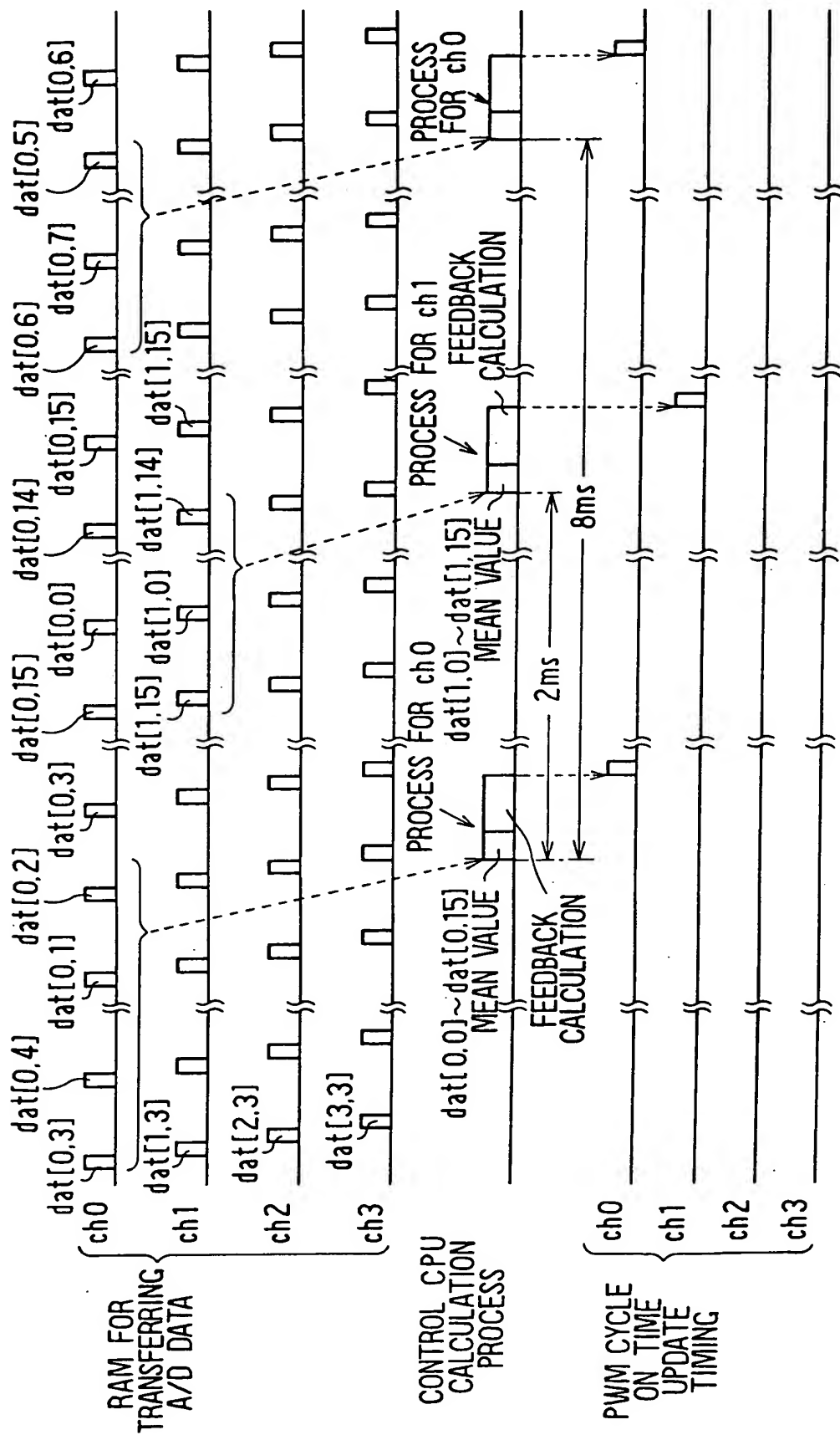
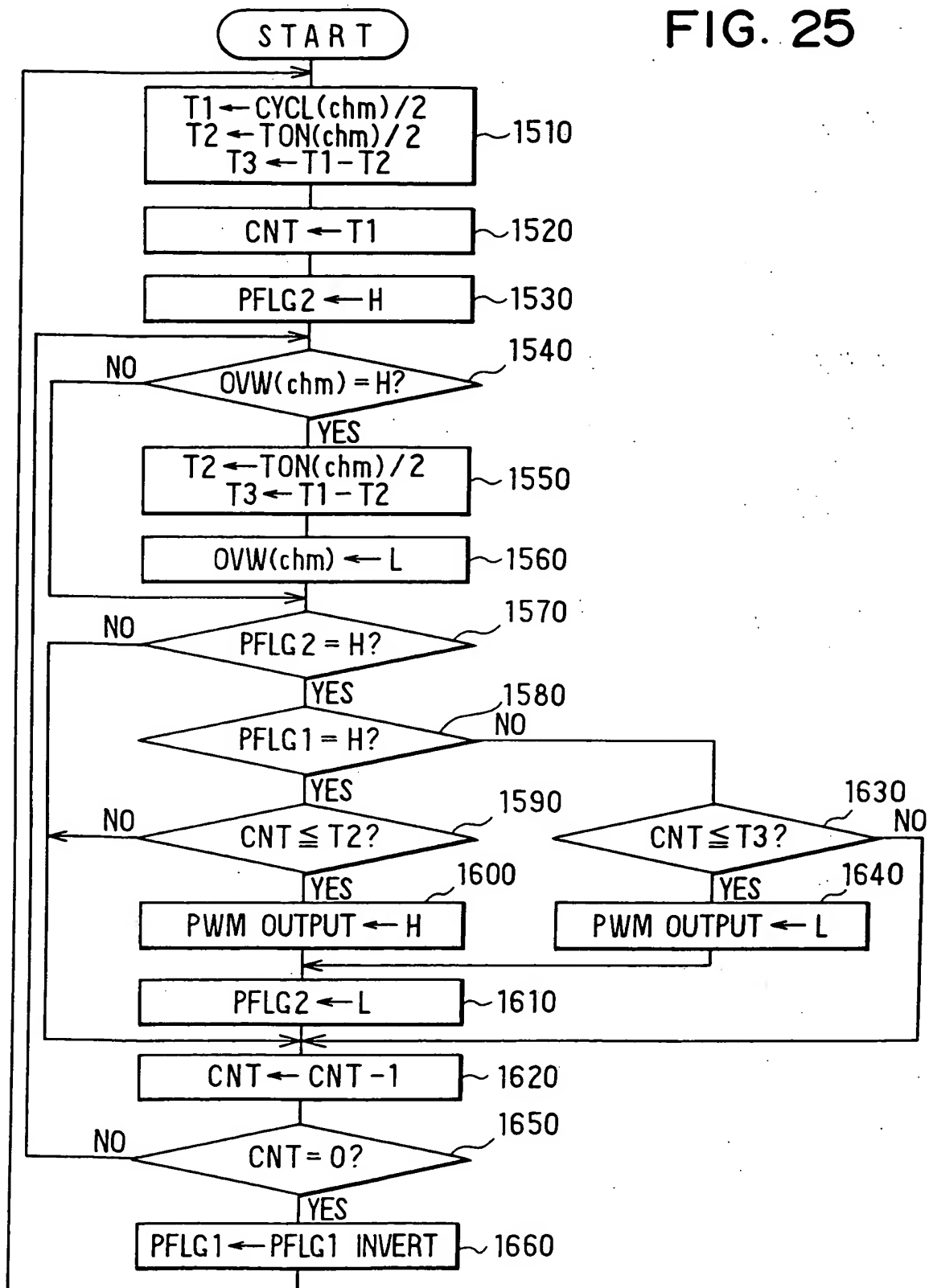
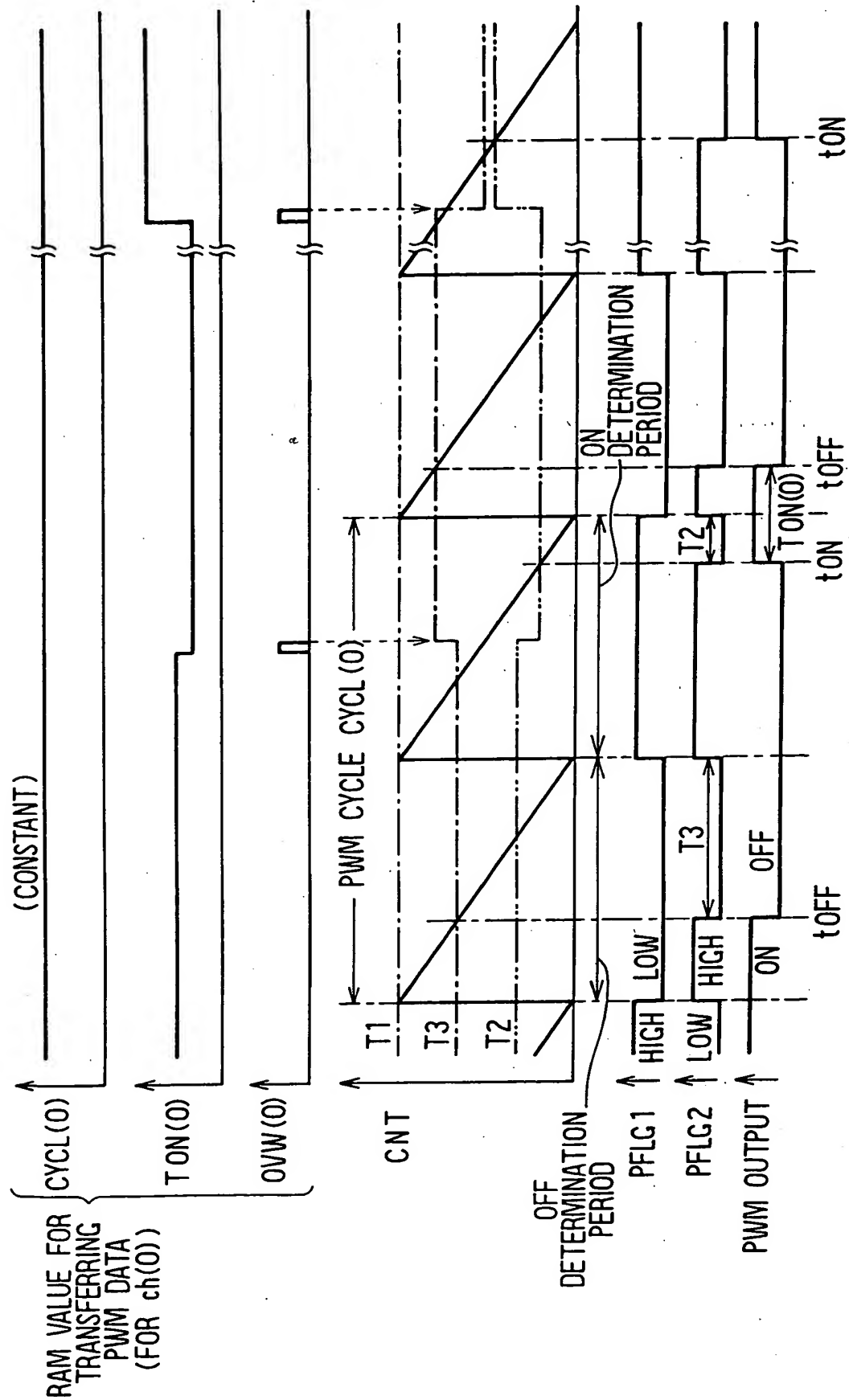


FIG. 25







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FIG. 27A

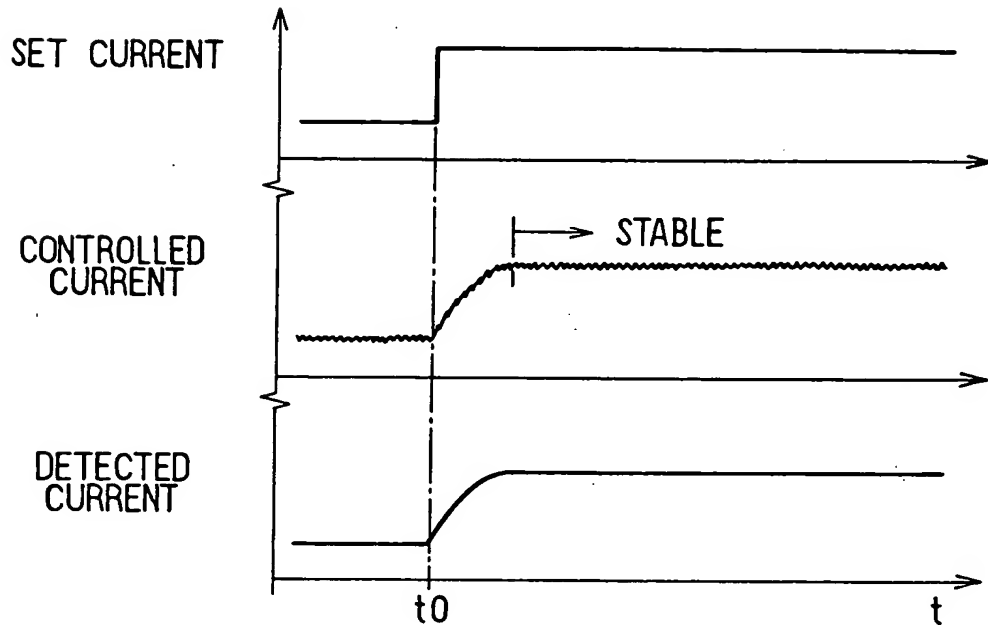
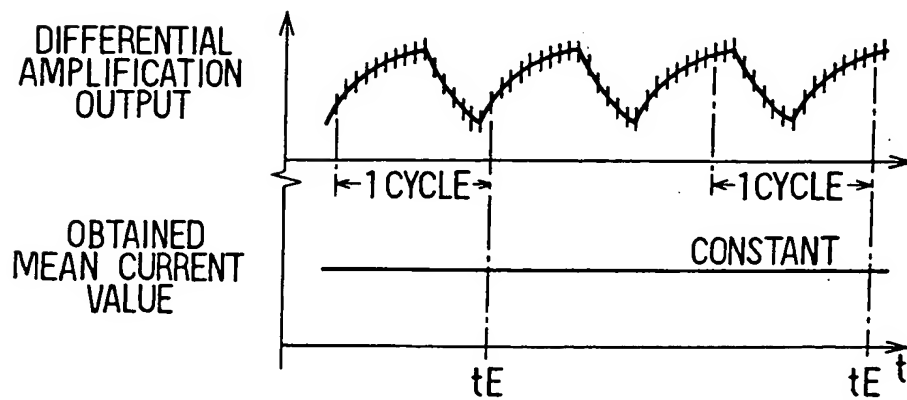


FIG. 27B



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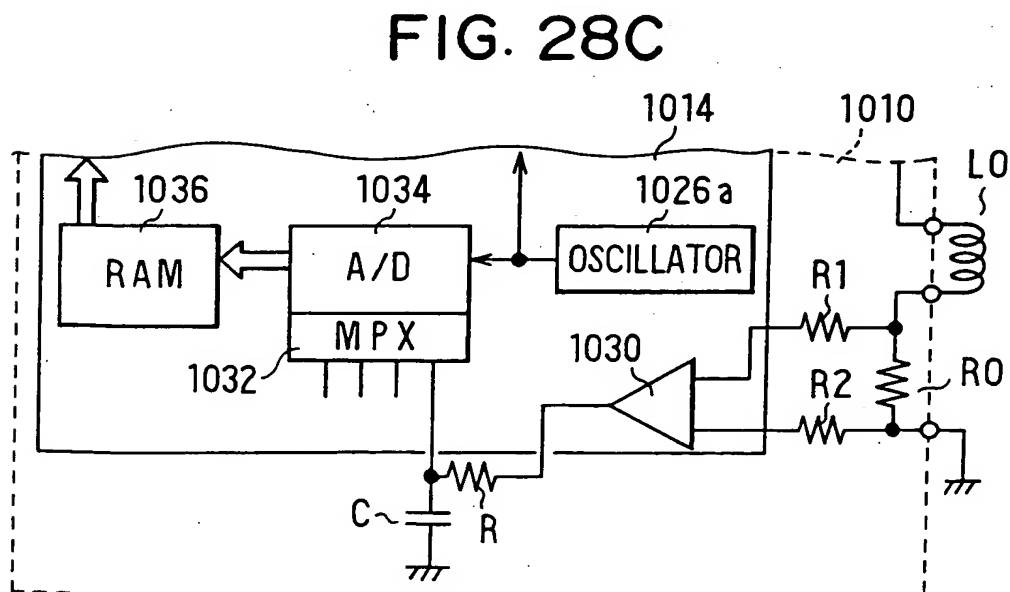
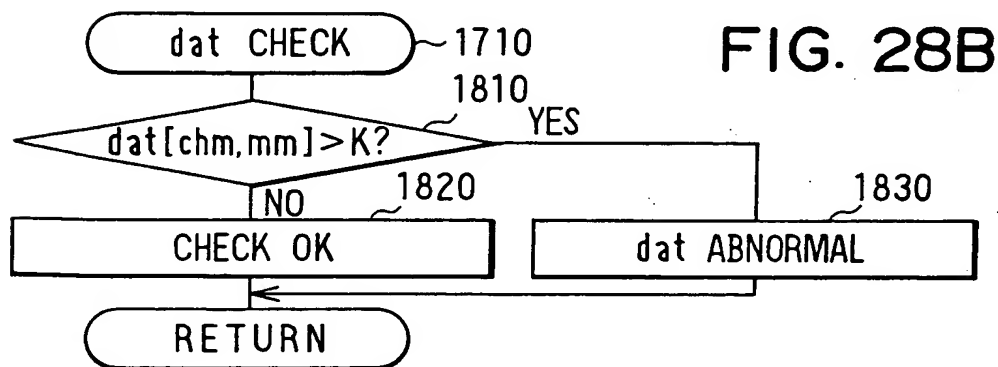
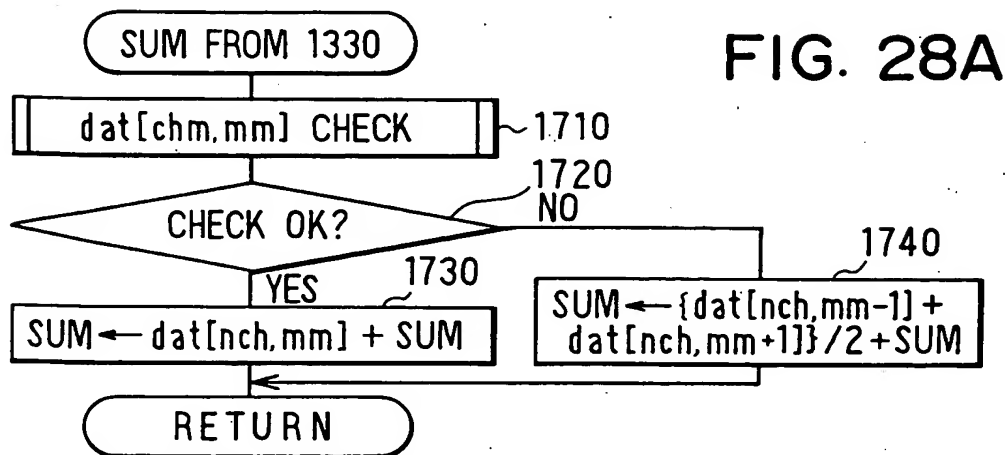
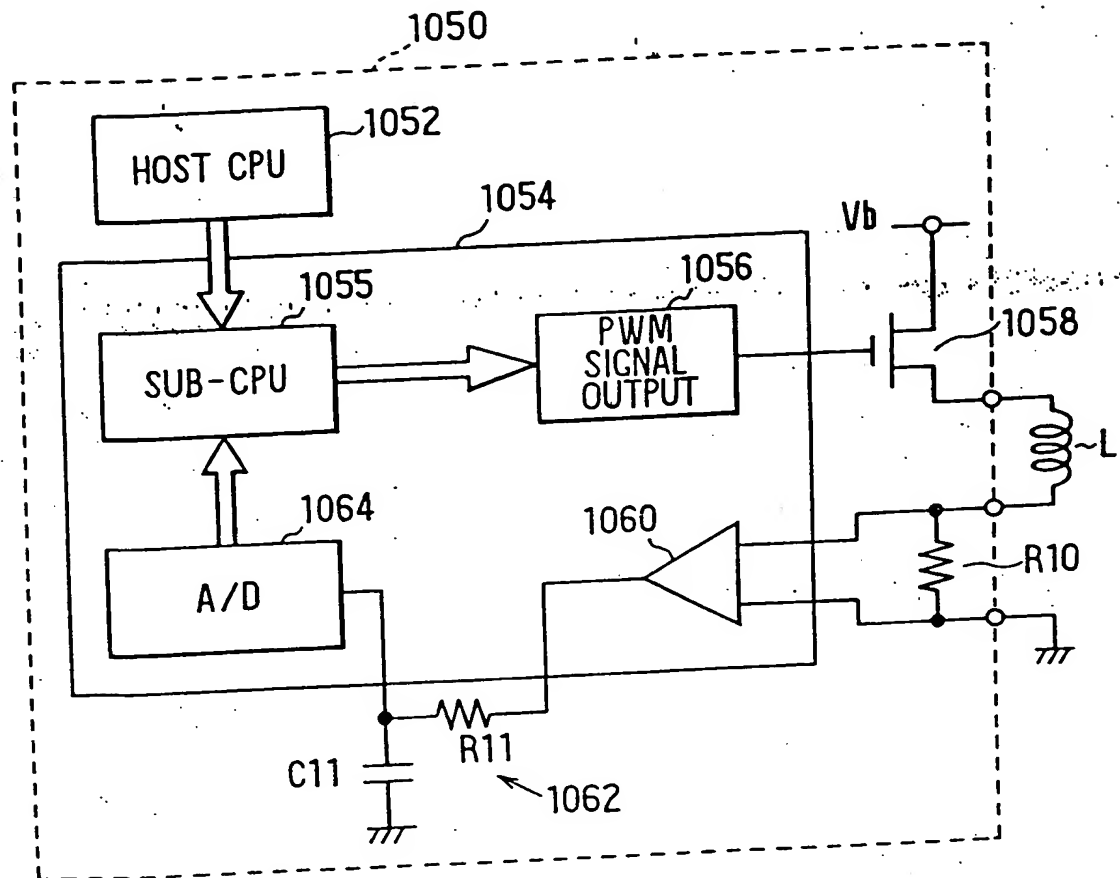


FIG. 29 PRIOR ART



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FIG. 30A PRIOR ART

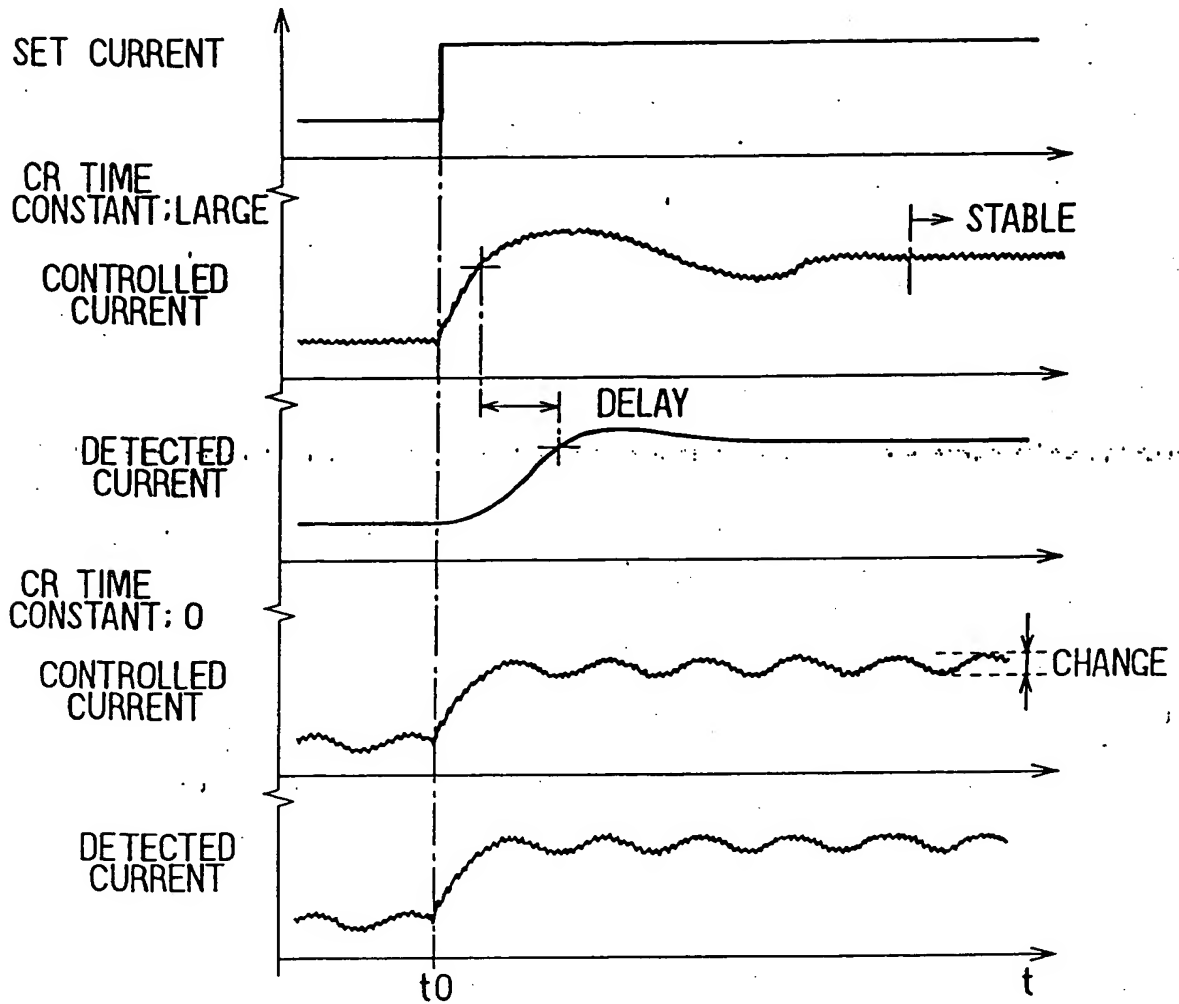


FIG. 30B PRIOR ART

